2023

COMPUTER SCIENCE — HONOURS

Paper : DSCC-1

Full Marks : 75

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

1. Answer ***any five*** questions : 2×5

(a) Convert decimal 478 to a 16-bit binary number by first converting to hexadecimal.

(b) Draw the circuit diagram to implement the expression $x = (A+B).(\overline{B} + D)$ using two input NAND gates only.

(c) Draw the Karnaugh map for the following Boolean expression :

$X = \overline{A}.\overline{B}.\overline{C}.\overline{D} + \overline{A}.\overline{B}.\overline{C}.D + \overline{A}.B.\overline{C}.D + A.\overline{B}.C.D + A.B.C.$

(d) Highlight four main differences between Assembly Language and High-level Language programming.

(e) Draw the logical circuit diagram of 2 to 1 multiplexer designed using fundamental logic gates.

(f) What is the highest clock frequency that a 6-bit asynchronous up counter can support, given that each flip-flop in it has a propagation delay of 50 nanoseconds?

(g) What does the term 'race around condition' refer to in relation to flip-flops?

(h) How can you implement an XNOR logic function using just five two-input NAND gates? Illustrate the necessary circuit diagram.

Answer ***any three*** questions.

2. Simplify the Boolean expression

$Y = \overline{A}.\overline{B}.C + \overline{A}.B.\overline{C}.D + A.\overline{B}.C.D + A.B.C.D. + A.B.C.\overline{D}$ using Karnaugh map and realise the simplified expression using fundamental logic gates. Draw the appropriate circuit diagram. 5

3. How can you configure 4-to-1 multiplexers in a cascade arrangement to create a 16-to-1 multiplexer? Include the truth table and briefly describe its operation. No other logic gates are allowed to realise the circuit. 5

4. Draw the circuit diagram of a TTL NOT gate and provide a brief explanation of how it operates. Define floating input with respect to TTL Logic gates. 4+1

5. Illustrate the circuit diagram for a clocked JK flip-flop, provide a concise explanation of its operation, and include its truth table. 5

6. Compose a brief note on ***any topic*** of your choice : 5×1

   (a) Primary memory and Secondary storage devices

   (b) Central Processing Unit

   (c) General characteristics of Supercomputers.

Answer ***any five*** questions.

7. Design a 3-bit synchronous up counter that sequentially progresses through the states : 000 — 010 — 100 — 110, and then repeats. Illustrate the state transition diagram and outline the requisite design steps, including the suitable logic circuit diagram. 6+2+2

8. Design a Master-Slave flip-flop utilizing JK flip-flops. Develop the truth table, elucidate its functionality, and depict the logical circuit diagram. 4+3+3

9. Design a BCD to Excess-3 code converter. Provide a truth table, simplify it using a Karnaugh map, and illustrate the logical circuit diagram using fundamental logic gates. 3+2+3+2

10. Realize the logic function, $F(A, B, C, D) = \Sigma_m(1, 3, 5, 7, 9, 11, 13)$ employing a 3 : 8 decoder featuring active-low outputs. Utilize additional basic logic gates as necessary. Draw the truth table. Describe the design procedure. Draw the logical circuit diagram. 4+3+3

11. What is a full adder? Illustrate its truth table, derive simplified expressions for the Sum and Carry out, and depict the logical circuit diagram. 3+3+2+2

12. Describe the functionality of a 3-bit Johnson counter using an appropriate illustration. 6+4

13. Convert a D flip-flop into a JK flip-flop. Illustrate the excitation table, elucidate the conversion process, and provide the logical circuit diagram. 3+4+3

14. Implement the function $F(A, B, C, D) = \Sigma_m(3, 4, 5, 6, 7, 9, 10, 12, 14, 15)$ using a 4 to 1 multiplexer along with other required logic gates. Explain the design process, create the truth table, derive the simplified expression, and provide the logical circuit diagram. 3+2+3+2