2023

COMPUTER SCIENCE — HONOURS

Paper : CC-1

(Digital Logic)

Full Marks : 50

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer ***question no.* 1** and ***any four*** questions from the rest.

1. Answer ***any five*** questions : 2×5

(a) Construct a XOR gate (2 input) using minimum number of two input NAND gates.

(b) What is principle of duality?

(c) What is S-R flip flop?

(d) What is SOP? Give suitable example.

(e) Convert the BCD number 0111 1100 0011 to its decimal equivalent.

(f) What is negative edge triggerred clock pulse?

(g) Simplify the boolean expression $x = A \cdot B \cdot C + A \cdot \bar{B}\left(\overline{A \cdot C}\right)$ and implement it using fundamental/basic logic gates.

(h) Design OR gate using 2-input NAND gates.

2. (a) What is a 3-bit full adder? Draw the truth table of a full adder. Derive the boolean expression for sum output and carry output from the truth table. Draw the logical circuit diagram using basic logic gates.

(b) Show that XOR gate can be used as control inverter. Give appropriate examples. (2+2+2+2)+2

3. (a) Draw the logic circuit diagram of master slave J-K flip flop using NAND gates and explain its operation and also draw the truth table.

(b) State and prove De-Morgan's theorem with appropriate example. 7+3

4. (a) Simplify the logic expression $F = \sum_m (1,4,6,8,9)$ using K-map. Draw the truth table and implement the simplified expression using basic logic gates.

(b) What is race-around problem? Give examples. 7+3

5. (a) Design a 3-bit full subtractor using two 4×1 multiplexers and other logic gates. Draw the truth table.
   (b) Draw the logical circuit diagram of a de-bouncer circuit using two input NAND gates. 6+4

6. (a) Implement a half adder using 4 to 1 multiplexer and other necessary logic gates. Explain the desig and draw the appropriate logic circuit diagram.
   (b) Realize XOR logic using NAND logic gates. 6+

7. (a) Construct a decade up 4-bit ripple asynchronous counter using J-K flip flop and explain its operati with appropriate illustration.
   (b) What is even parity generator? 8

8. Write short notes on (***any two***) : 5
   (a) TTL two input NAND gate
   (b) Universal shift register
   (c) Johnson Counter
   (d) Seven Segment display.
