2023

COMPUTER SCIENCE — MDC

Paper : CC-1

Full Marks : 75

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer **question no. 1** and **any three** questions from **Section - A** and **any five** questions from **Section - B**.

1. Answer **any five** of the following : 2×5

   (a) Write two differences between low-level and high-level languages.

   (b) Find out the octal representation of $(1F5 \cdot A2)_{16}$.

   (c) Prove that $X + Y \cdot Z = (X + Y) \cdot (X + Z)$, where X, Y and Z are Boolean variables.

   (d) Design a two input AND gate using a 2×1 multiplexer.

   (e) What is a common anode type seven segment display?

   (f) State the advantages of using synchronous counters over asynchronous counters.

   (g) Mention the differences between sequential and combinational circuits.

   (h) What is Delay flip-flop?

Section - A

2. Explain the working of a 4-bit binary adder-subtractor circuit with a neat diagram. 5

3. What is a magnitude comparator? Design a 1-bit comparator using NAND gates. 2+3

4. Convert a D flip-flop into a JK flip-flop. 5

5. (a) What do you mean by manchester code?

   (b) What are the differences between weighted and non-weighted code?

   (c) Convert $(9CB)_{16} = ( )_2$? $= ( )_8$? 1+2+2

6. (a) Design a D flip-flop.

   (b) Convert it to Toggle flip-flop. 3+2

Please Turn Over

Section - B

7. (a) Define half adder.

   (b) Implement a full adder using two half adders.

   (c) Why do we call decoders as min-term generators? Explain with an example. 2+3+5

8. (a) State De-Morgan's theorems.

   (b) Convert into canonical POS. Y = AB + BC.

   (c) Simplify the expression given below and draw the diagram by NAND gates :

   $$Y = \Sigma_m(1, 2, 6, 7, 8, 13, 14, 15) + \Sigma_d(0, 3, 5, 12).$$ 2+3+5

9. (a) Define full subtractor.

   (b) Implement a full subtractor using a 4×1 multiplexer.

   (c) Why demultiplexers are called data distributors?

   (d) Design an even parity checker. 2+3+3+2

10. (a) Subtract 24_{10} from 14_{10} by 2's Complement method.

    (b) Fill in the blank : $(17)_{10} + (21)_8 - (0F)_{16} = (?)_2$.

    (c) State the differences among Super, Mainframe, Mini and Personal Computer. 3+3+4

11. (a) Define propagation delay and noise margin in a logic gate.

    (b) Convert $(10110111)_2$ into gray code.

    (c) Design a Johnson Counter using D flip-flops. 4+2+

12. Design 32 to 1 multiplexer using 8 to 1 multiplexers. — Explain with truth table. 1

13. (a) Design a priority encoder using basic logic gates and give the truth table.

    (b) Realize a 2 to 4 decoder using NAND logic gates. 5+

14. (a) What is the truth table of a JK latch? From that deduce the characteristic equation, hence draw JK latch using NAND gates.

    (b) Define the race around condition of JK flip-flop and hence explain how master-slave JK flip-fl overcomes this issue. 5-